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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Bezeichnung der Erfindung: Title of the invention: Titre de l'invention:
A wafer scale package, a camera module, a camera system, a system of manufacturing a camera module, a method of manufacturing a solid spacer layer for use in a camera module, and a method of manufacturing a tranparent cover layer

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A wafer scale package, a camera module, a camera system, a method of manufacturing a camera module, a method of manufacturing a solid spacer layer for use in a camera module, and a method of manufacturing a transparent cover layer

The invention relates to a wafer scale package according to claim 1, a camera module according to claim 16, a camera system according to claim 32, a method of manufacturing a camera module according to claim 33, a method of manufacturing a solid spacer layer for use in a wafer scale package according to claim 36, and a method of manufacturing a transparent cover layer for use in a wafer scale package according to claim 39.

Today's developments in image sensor technology are paving the way for a new generation of digital imaging products with broad consumer applicability. According to research studies, consumer's first preference for a computer peripheral is a digital camera. Digital camera sales are continuing to boom since this high quality, full-featured products become affordable for a broad base of consumers. With the ability to provide instantly viewable and easily insertable images into computer-generated documents, the rise in the popularity of the Internet as a communications medium, and most importantly, the elimination of the cost and time of film processing, digital cameras are going to replace traditional film cameras for many consumer applications. The total available market for digital imaging, including industrial and security cameras, medical appliances, automotive sensors, PC video cams, scanners, digital still cameras and digital camcorders is forecasted to grow from about 20 million units in 1996 to over 100 million units in 2002. Thus, though competition in the market demands for more efficient and rationalized manufacture of image sensor devices for the mass consumer market.

In a nutshell, image sensors, also called imaging devices or simple imagers, are specialized integrated circuits that act as eye of electronic equipment. Thereby, these detect and convert incident electromagnetic radiation, preferably light, i.e. photons, first into electronic charge, i.e. electrons and, ultimately, into digital bits, i.e. binary information. Each individual picture element, also called pixel, corresponds to a solid-state photosensitive electrical sensor element. Typically, an image sensor comprises at least in a row of such sensor elements, e.g. in scanners. Usually, these sensor elements are arranged as a two-dimensional matrix forming a photosensitive area, preferably being located at an image plane of the image to be converted. Such image sensors can be found for instance in digital still or

video cameras. The side of the chip containing the sensor elements which functions as the photosensitive area will herein be referred as to the sensor side.

As to the photosensitive electrical sensor elements, there are two major technologies, the Charge Coupled Device (CCD) technology and the Complementary Metal Oxide Semiconductor (CMOS) technology. As to the first, simplest CCD image sensor element imaging one pixel is a charge transfer device that collects photocharge in pixels and uses clock pulses to shift the charge along a chain of pixels to a charge-sensitive amplifier. CCD's output pixel-by-pixel analog signals, which are ultimately digitized. As to the latter, simplest CMOS image sensor element imaging one pixel is a passive pixel, which consists of a photodiode and an access transistor. The generated photocharge within the photodiode is passively transferred from each pixel to downstream circuits.

As to the image sensor performance, an important aspect in imager sensors is the fraction of real estate within each pixel, which detects light, i.e. the optical fill factor. Today's fill factors do not reach 100% since a pixel area's part is used for signal transfer to the rest of the imager circuits. Therefore, light falling elsewhere is either lost or may create artifacts in images by generating electrical currents in the circuitry. Accordingly, micro lenses can be applied to increase fill factor and meet higher performance objectives. Micro-lenses, nowadays standard feature of CCD and CMOS image sensors, may be etched directly in a transparent layer of a suitable material applied on the chip's surface for each pixel or added separately as an individual element during manufacture. In operation, they focus light on each respective pixel's photosensitive part and thus, when accurately deposited over each pixel, concentrate the incoming light into the photosensitive region and increase so effective fill factor. For effectiveness, micro lenses need a difference between the refraction index of the micro lens material and at least the refraction index of air. That is, micro lenses need an air gap to take advantage of the light fraction caused by the difference between the refraction of the micro lens material and the air within the air gap. However, since such air gap is generated during the final manufacturing of imager modules, a significant problem is pollution of the photosensitive elements by alien materials.

Moreover, since a Solid State Image Sensor device needs an optical system for projecting a desired image onto the photosensitive area, there are different problems in assembling and mounting of such optical systems onto the sensor side. In a first step a glass layer may be to be glued onto the wafer containing the integrated image sensor circuitry. However, commonly used adhesives have nearly the same refraction index as the micro lens material so that the effect of the micro lenses will be neutralized. Thus, contact between the

adhesive and the micro lenses has to be avoided. Secondly, there are a lot of parameters influencing the focus of a optical system, for instance the optical system has to be carefully aligned with the photosensitive area, plus there should be no tilt between the optical system's image area and the photosensitive area, further, it is crucial to have control of the heights within the lens system with respect to the photosensitive area to avoid costly individual focusing of each image sensor. In this regard, a major target of actual research is going on wafer level packing (WLP), i.e. to concentrate as much as possible steps of imager module production at wafer scale.

US-Patent 6,285,064 discloses a chip scale packing for optical image sensor integrated circuits, wherein micro lenses are placed on top of a wafer having the image sensors formed thereon. An adhesive matrix is placed atop of the wafer. The adhesive matrix has openings that align with the micro lensed sensor array on top of the wafer. A cover glass is then placed over the adhesive and the adhesive is activated to secure the cover glass to the wafer. Because the adhesive has openings above the micro lensed portion distortion or reduction of the lens effect by the adhesive shall be avoided. However, it is hard to control the distance between the image area and the cover glass, also is it possible that the cover glass wafer is not exactly parallel with respect to the wafer having the image sensors formed thereon. In such case, nearly each individual die will be different.

It is inter alia an object of the present invention to provide a wafer scale package that provides an improved control of the distance between the image area and a transparent cover layer. This object is achieved by means of a wafer scale package comprising: a wafer with a sensor side, comprising a plurality of image sensor integrated circuits said image sensor integrated circuits having a photosensitive area located near said sensor side, comprising photosensitive elements for converting electromagnetic radiation to electric signals, a solid spacer layer being arranged over said sensor side of said wafer, having a plurality of openings corresponding to the photosensitive areas, said openings preferably having at least the same areal dimensions as said photosensitive areas, a transparent cover layer being arranged over said spacer layer.

The thickness of the spacer layer can be defined with a very narrow tolerance. By changing the thickness of the spacer layer, the distance between the transparent cover layer and the sensor side of the waver can be defined accurately.

In a preferred embodiment of the wafer scale package according to the invention said cover layer comprises optical means, preferably a plurality of lenses each corresponding to one of said photosensitive areas, arranged for modulating electromagnetic radiation through said optical means to said photosensitive areas.

This results in a wafer scale package that includes both the solid state image sensors and the optical means for projecting images on the photosensitive areas of the image sensors. The advantage of this wafer scale package is that is height is limited. Thus after separating the wafer scale package into individual camera modules, for instance by dicing, the physical dimensions of the resulting camera modules will be small. This makes these very suitable for use in applications such as for instance cellular phones or PDA's, where physical dimensions usually need to be as small as possible.

A further preferred embodiment of the wafer scale package according to the invention comprises a further transparent cover layer being arranged over said transparent cover layer. Preferably the wafer scale package comprises a further spacer layer having a plurality of further openings corresponding to the photosensitive areas, said further openings having at least the same areal dimensions as said photosensitive areas. Preferably at least one of said cover layers comprises optical means arranged for modulating electromagnetic radiation traveling through said optical means to said photosensitive areas.

In such a wafer scale package it is possible to add additional features and still maintain a package with a limited height. For instance a first cover layer may be used to create an accurately defined air gap to the sensor side of the wafer. This may be useful in case the sensor side is covered with micro lenses. For an optimal performance of these micro lenses such an accurately defined air gap is desirable. Furthermore the first layer may be made of infra red blocking glass or may be covered with an infra red blocking coating. Usually solid state image sensors utilize silicon photo sensitive elements. These have a high sensitivity for electromagnetic radiation in the infra red part of the spectrum. Using infra red blocking means may be utilized to improve the performance of the photosensitive elements in the visible light part of the spectrum. A second cover layer may comprise the optical means for projecting images on the photosensitive area of the image sensor in operation. Alternatively both cover layers may comprise optical means. Using two lenses in the optical

part may result in a better alignment of the focal plane with the plane where the photosensitive area is located in.

A camera module according to the invention comprises a semiconductor material die with a sensor side, comprising an image sensor circuit, said image sensor integrated circuit having a photosensitive area located near said sensor side, comprising photosensitive elements for converting electromagnetic radiation to electric signals, a solid spacer layer being arranged over said sensor side of said die, having an opening corresponding to said photosensitive area, said opening preferably having at least the same areal dimensions as said photosensitive area, a transparent cover layer being arranged over said spacer layer. Using a solid spacer layer has the advantage that the thickness of the spacer layer can be defined with a very narrow tolarance. By changing the thickness of the spacer layer, the distance between the transparent cover layer and the sensor side of the waver can be defined accurately.

The thickness of the spacer layer can be defined with a very narrow tolarance. By changing the thickness of the spacer layer, the distance between the transparent cover layer and the sensor side of the waver can be defined accurately. A further advantage of the camera system according to the invention has the advantage that it can be small, because its area or footprint on a PCB is determined by the size of the comprising the solid state image sensor circuit, while its height is mainly determined by the height of the stack of said layers. This is very important for use in applications such as for instance cellular phones or PDA's, where physical dimensions usually need to be as small as possible.

A camera system according to the invention has a camera module comprising: a semiconductor material die with a sensor side, comprising an image sensor circuit, said image sensor integrated circuit having a photosensitive area located near said sensor side, comprising photosensitive elements for converting electromagnetic radiation to electric signals, a solid spacer layer being arranged over said sensor side of said die, having an opening corresponding to said photosensitive area, said opening preferably having at least the same areal dimensions as said photosensitive area, a transparent cover layer being arranged over said spacer layer.

The camera system according to the invention has the advantage that it can be small, because the camera module applied in the camera system can be small. This is very important for use in applications such as for instance cellular phones or PDA's, where physical dimensions usually need to be as small as possible.

A method of manufacturing a camera module according to the invention, whereby said camera module comprises a semiconductor material die with a sensor side, comprising an image sensor integrated circuit having a photosensitive area near said sensor side, said photosensitive area comprising photosensitive elements for converting electromagnetic radiation into electric signals, comprises a separation step of separating said die from a wafer, said separation step being preceded by a spacer layer arranging step of arranging a solid spacer layer over said sensor side of said die, said solid spacer layer having an opening corresponding to said photosensitive area, said opening preferably having at least the same real dimensions as said photosensitive area, said spacer layer arranging step being followed by a step of arranging a transparent cover layer over said spacer layer.

An advantage of the method according to the invention is that it results in a better controlled manufacturing process. The complete manufacture up to the separation of the camera modules from the wafer scale package is at the wafer level. This simplifies handling during production. Furthermore since the layers are glued on the wafer and the tolerances within the focussing direction are very small, there is no need for a focus adjustment, i.e. the heights within the optical system may be controlled to a high degree. In existing camera modules based on solid state image sensors, the lens or lenses may be tilted with respect to the die, leading to a degraded projection of the electromagnetic radiation on the photosensitive area. By use of the method according to the invention the optical system will be aligned in parallel to the photosensitive area.

A method of manufacturing a solid spacer layer for use in a wafer scale package according to the invention, comprises a step of forming an array of openings in said spacer layer. Using a solid spacer layer has the advantage that the thickness of the spacer layer can be defined with a very narrow tolarance. This may be advantageously applied in a camera module comprising a die with a sensor side, said die comprising an image sensor integrated circuit having a photosensitive area, comprising photosensitive elements for converting electromagnetic radiation to electric signals. Such photosensitive areas are preferably covered with a plurality of micro lenses, each of said micro lenses corresponding to a photosensitive element. For a proper functioning of said micro lenses a well defined air gap between a transparent cover layer and the micro lenses is required. This may be obtained by mains of the spacer layer according to the invention. By changing the thickness of the spacer layer, the distance between the transparent cover layer and the sensor side of the die can be accurately controlled.

A method of manufacturing a transparent cover layer for use in a wafer scale package according to the invention, comprises a step of forming an array of lenses in said cover layer. Lenses required in camera modules comprising image sensor integrated circuits add to the cost price of these camera modules. Using the method according to the invention results in lenses with well defined, reproducible optical properties. Since the lenses are manufactured on a wafer scale, handling during production is simplified and the production process is simplified. The method thus results in good quality lenses manufactured at a lower cost prices, because the production process is simplified. This helps in reducing the overall manufacturing costs of the camera modules and thus of an entire camera system, for instance a cellular phone or a PDA.

Furthermore because of the wafer scale manufacturing of the lenses the placement of the lenses within the camera modules may also by simplified, because this may done while the camera modules are still part of a semiconductor material wafer.

A first aspect of the present invention is directed to the air gap for micro lenses. In case, said photosensitive area of a SSIS die is recessed with respect to surface of said sensor side, micro lenses may by applied to said photo sensitive area and over the micro lensed photosensitive area a cover glass sheet, i.e. said first transparent layer, can be applied. Due to the photosensitive area being recessed with respect to the surface of the SSIS'S sensor side an air gap is formed. In the other case, said photosensitive area within said sensor side is not recessed with respect to the surface of said sensor side, the photosensitive area of the SSIS's sensor side will also be micro lensed. Advantageously, the air gap is made by using two glass sheets, preferably having wafer size, one with through holes, i.e. said spacer layer, having the same size of the image array and one normal cover glass sheet, i.e. said first transparent layer. The two glass sheets, i.e. said spacer layer and said first transparent layer, are bonded or glued together. Then both are glued with the spacer layer side onto the silicon wafer. This results in creating an air cavity above the micro lenses. By changing the thickness of said spacer layer the size, i.e. height, of the air cavity can be controlled. By this way imperfection within the glass can be shifted out of focus if said spacer layer is made thicker. As to the through holes within the spacer layer, these may be made by Ultra Sonic (US) drilling, powderblasting or etching.

As to a second aspect of the present invention, several arrangements for manufacturing the optical system, also called lens system, for a SSIS will be discussed in the following. However it should be noted that it goes without saying said the present invention should not be restricted to the following examples derived from the inventive basic idea.

Accordingly, the basic idea is to have layers, preferably for instance glass sheets, having wafer size. Some of these glass sheets containing an array of lenses, i.e. said transparent layers comprising optical means for modulating electromagnetic radiation, and glass sheets containing trough holes, i.e. said spacer layers, to be used as spacers between different glass sheets with lenses. From these two kinds of layers a stack can be built which will form a wafer level optical system for the SSIS. Therefore, theses glass sheets are mounted onto the silicon wafer comprising an array of SSIS dies and then, the wafer can be sawed into round about 1000 SSIS modules (8" wafer). Since lenses are the expensive part of existing SSIS modules, with the present invention a high cost reduction in manufacture of these modules can be achieved.

In first approach the basic idea of the present invention will be sketched by a first and a second embodiment: in the first embodiment according to the present invention, a single lens array is mounted on the wafer. However, in this solution the focal plane is curved, this means the focus points, i.e. the crossing of the light rays, on the edges of the photosensitive area of the die do not reach the surface of the photosensitive area. This leads to a low performance regarding MTF of the optical arrangement. As second embodiment, a second spacer layer is arranged between said first and said second transparent layer. This solution has more or less the same performance as the first embodiment.

In a third embodiment, a additional glass sheet with lenses, i.e. a third transparent layer comprising optical means for modulating of electromagnetic radiation traveling through said optical means to said photosensitive area, is arranged between said first and said second transparent layer. This means a stack of layers comprising at least two layers with an array of lenses an one spacer layer are combined. In this embodiment, assumed that only convex lenses are used, there are three different combinations to build a wafer level optical system. As to the first and second arrangement, the stack is built that adjacent to the first transparent layer comes the third transparent layer with lenses, adjacent to this follows a spacer layer, and on top is the second transparent layer with lenses. In this arrangement, for orientation of the lenses in the second transparent layer there are two possibilities: with respect to the convex lens, the lens can be turned towards or away from the photosensitive area. As third possible arrangement, the spacer layer is mounted next to the first transparent layer and on top follow the third and the second transparent layer with lenses, respectively. Since these both final layers have to be fixed together there is only on possible arrangement. The lens contained in the third transparent layer is orientated towards the die and the lens in the second transparent layer is turned away from the die. In other words, both lenses are

turned away from each other. All three combinations have good optical performance because the combination of two lenses works as a combination of a lens and field flatter. The very first arrangement has proved to be preferred since here the lowest height from all three can be achieved, furthermore, a large chief angle for the incoming electromagnetic radiation, preferably light, can be used in the cavity between the two lenses.

As to the cost reduction aspect of the invention, due to complete manufacture on wafer level a high impact on the production cost can be provided. However, there are other advantages as well. Since the layers are glued on the wafer and the tolerances within the focusing direction are very small, there is no need for a focus adjustment, i.e. the heights within the wafer level optical system can be controlled to a high degree. In existing modules for comparison, the lens and the die can be tilted which will lead in the output pictures to shading of sharpness since the focus plane is not parallel to the photosensitive area on the die surface. With the present invention the optical system will be parallel so that the tilt error can be reduced to nearly zero. A further problem of the existing modules is the alignment of the optical center of the optical system with the optical center of the photosensitive area, i.e. the middle image, on the die surface. For manufacture on wafer level, i.e. WLP, there exist techniques to align two wafers accurate within a few micrometers. At this moment, the alignment is about 100 micrometers. Since lens performance drops to outer sides, recognizable as vignette, i.e. the image shades off gradually into the surrounding, and as increasing error in the lens's MTF, i.e. sharpness is degrading, accurate placement off the layers is very crucial. Moreover, existing modules have plastic lenses and thus, may not be heated over 80°C. As a standard technique to place and assemble components on a PCB reflow soldering is known. However, this process has peak temperatures of about 240°C. This means reflow soldering can not be used for assembling today's modules. With the introduced glass layer stack process according to the present invention this will be possible.

It should be noted that one of the transparent layers or an additional transparent layer can be made of IR glass. Advantageously, infrared radiation contained within the normal light spectrum is prevented from reaching the integrated circuitry of the SSIS. Thus, performance of the SSIS is not harmed by warming up.

In a further development of the present invention, it may be desirable to have a diaphragm within the wafer level optical system. Such diaphragm will enhance the optical performance of the wafer level optical system for the SSIS. According to the individual application, such diaphragm may be adapted to the desired depth of focus, e.g. a high depth of focus is applicable in all applications where the object to capture is not within a fixed

distance to the photosensitive area. With respect to the present invention, a diaphragm can be provided easily by an additional diaphragm layer to the stack of layers forming the wafer level optical system. The diaphragm layer will be made of on opaque material, wherein opaque means that it is not transparent for the electromagnetic radiation which is captured by the wafer level optical system to be projected onto the photosensitive area of the SSIS.

According to a further embodiment of the present invention, said second transparent layer is a wafer level lens holder and optical means for modulating electromagnetic radiation traveling through said optical means to said photosensitive area are placed within said wafer level lens holder. The wafer level lens holders may also be made of glass, preferable for WLP it is made from a glass sheet having wafer size. In this glass sheet cavities are made, in which optical lenses can be placed as means for modulating electromagnetic radiation. These cavities may be generated by use of very fine sandblasting or powderblasting. The same method as used for generating a spacer layers, e.g. between the SSIS die and the cover glass.

As to the mounting of SSIS on wafer level, such process may comprise the following: at first, the dies are packed. This packing on wafer level includes the installation of micro lenses and the cover glass sheet, i.e. said first transparent layer, and if necessary said spacer layer. Onto the cover glass an IR glass layer can be mounted for damping infrared radiation. On top of the IR glass layer now the wafer level lens holder is placed. This placing can be done with great accuracy, since methods for alignments on wafer level are well known. This means that ones the wafer level lens holder is in right position all cavities for receiving the lenses are in right position, i.e. coinciding with the respective photosensitive area of each SSIS contained on the wafer. After the wafer level lens holder is glued to the IR glass the lenses can be mounted into the cavities of the wafer level lens holders. After mounting the lenses the modules are separated to single modules, which can further be mounted to a flex foil for better interconnection. In case that all layers are made of glass the final SSIS module needs for a sunshade. Such a sunshade can be mounted before installation into an application, or be a part of the housing in which the SSIS module will be installed.

The above and other objects, features and advantages of the present invention will become more clear from the following description of the preferred embodiments thereof, taken in conjunction with the accompanying drawings. It is noted that through the drawings same or equivalent parts remain the same reference number. All drawings are intended to illustrate some aspects and embodiments of the present invention. Devices and manufacture steps are depicted in a simplified way for reason of clarity. Not all alternatives and options

are shown and therefore, the present invention is not limited to the content of the accompanying drawings.

In the following, the present invention will be described in greater detail by way of example with reference to the accompanying drawings, in which:

Fig. 1 shows according to a first aspect of the present invention a slice plane of a wafer with micro lensed SSISs dies and an air gap formed by combination of a spacer layer and a cover glass layer;

Fig. 2a – 2d illustrate according to a second aspect of the present invention slice planes of wafers with SSISs which demonstrate arrangements of the layer stack forming a wafer level optical system;

Fig. 3a – 3d represent simulations of different wafer level optical systems; and

Fig. 4a – 4e chart a SSIS wafer level packing process according to a further embodiment of the present invention.

Fig.1 shows a slice plane of a part of a silicon wafer 10, comprising an array of SSIS dies (not illustrated in Fig.1). There are micro lenses 12 mounted onto the photosensitive area of each individual SSIS die. To provide an air gap for the micro lenses 12, according to the present invention, there is a spacer layer 20, which is glued or bonded together with a glass layer 30, attached to the silicon wafer 10. Additionally, there are illustrated dicing lines S, in Fig.1, where the final wafer level packed SSIS modules will be diced into single SSIS modules.

In Fig.2a to 2d show, in way of slice planes as in Fig.1, different arrangements for the wafer level optical system for an SSIS, according to the principle of the present invention. All through the Fig.2a to 2d there is a silicon wafer 11, comprising an array of SSIS dies (not illustrated in Fig. 2a to 2d) and a covering glass layer 31, preferable made of an IR glass. For better illustration, there is only shown a section of the whole wafer, what is indicated by the doted line on the left side of each Fig. 2a to 2e. It will be noted that within the arrangement of the silicon wafer 11 and the glass layer 31, there may be attached lenses to the photosensitive area of the SSIS dies according to the detailed illustration of Fig.1. As to the performance of the introduced wafer level optical systems, to this will be referred together with Fig.3a to 3d.

The wafer level optical system in Fig.2a only comprises the first glass layer 31 and a second glass layer providing convex lenses 50 orientated away from surface of the silicon wafer 11. In Fig.2b there is the only change in comparison to Fig.2a that a spacer layer 22 has been inserted between the first transparent layer 31 and the second transparent layer 40 containing the lenses 50. As to Fig.2c, there is a further minor change with respect to Fig.2b, here an additional glass layer 42 comprising lenses 52 has been inserted between the spacer layer 22 and the first glass layer 31. In this embodiment, there is an air gap between the two lenses 50, 52 of the wafer level optical system. Finally, Fig. 2d shows an arrangement, again in comparison to Fig.2b, wherein a additional glass layer 44 with lenses 54 is arranged between the spacer layer 22 and the glass layer 40.

Now reference is made to Fig.3a to 3d, here the performance of some examples for wafer level optical systems according to the present invention are illustrated by way of simulation diagrams. The simulations give results according to performance and dimensions of a wafer level optical system according to the present invention. All simulation diagrams read as follows: starting from the left, i.e. the real image which is to be projected by the optical system, there are light rays, which are depicted as lines, going through the optical system and crossing each other behind the optical system. The crossing points of these simulated light rays could be connected by a drawing line, this would lead to the ideal image plane wherein the real image would be projected without error. However, since the photosensitive area of a SSIS is flat, the wafer level optical system has to be adapted to a flat photosensitive area as image plane. Looking at Fig.3a shows that an optical system with only one lens has a very curved image plane and therefore, produces increasingly low performance towards the edges of the images plane. Fig.3b to 3d displays the advantage of a second lens within the optical system, since both lenses work together as to focus and as to flatten the image plane and thus, the image plane is more adapted towards the photosensitive area. The arrangement in Fig.3b has proved to be the best, since the arrangement is very low in height. This is due to the fact, that a large angle for the traveling light can be used in the air cavity between the two lenses.

Now reference is made to Fig.4a to 4e, here several steps of the manufacture process of a further embodiment of the present invention are illustrated. Since one major aspect of the present invention is a wafer level optical system for SSIS devices, Fig.4a starts at the stage where the dies are already packed. As can be seen from top of Fig.4a, there is mounted on the top side of the silicon wafer 15 the spacer layer 25 for the micro lenses (not illustrated in Fig.4a and b). In a next step a cover glass layer 35 is attached to the spacer layer

25. Onto the cover glass layer 35 is an IR glass layer 36 mounted. Till this point in manufacture, the SSIS dies are wafer level packed. Here follows a further step for installing an optical system for the SSIS on wafer level. Therefore, on top of the IR glass layer 36 a wafer level lens holder 60 with cavities 62 for lenses is placed. This leads to Fig.4b. Now referring to Fig.4c, after the wafer level lens holder 60 has been glued to the IR glass layer 36, the lenses 70 are mounted into the cavities 62 of the wafer level lens holders 60. In Fig.4d can be seen that the single SSIS modules are separated after mounting of the lenses 70. In a next step such a SSIS module 100 can be installed onto a flex foil 90 for interconnection. Furthermore, due to the reason that the whole SSIS module optical part consists of glass, there is a need for a sunshade 80. This sunshade 80 can be mounted before installation into an application or can be a part of a housing in which the SSIS module 100 can be installed.

The embodiments of the present invention described herein are intended to be taken in an illustrative and not a limiting sense. Various modifications may be made to these embodiments by persons skilled in the art without departing from the scope of the present invention as defined in the appended claims.

For instance although silicon is ideal for making active devices, it exhibits poor high frequency properties due to its semiconductor nature, there are poor interconnects and cross talk, and high-quality strip lines and inductors are hard to integrate. However, Silicon-On-Insulator (SOI) technology can be used as a new approach to enable semiconductor circuitry to be transferred to a range of insulating substrates. The advantage of using an insulator over silicon is that parasitic capacitances are reduced. A broader approach to SOI is so-called Silicon-On-Anything (SOA) technology. With SOA the complete circuitry is transferred to an insulating substrate such as glass and thus, the afore-mentioned negative effects can almost entirely be eliminated. In principle, the wafer containing functional electronic circuitry is glued top-down to another substrate and the original silicon is almost completely removed. At the moment, SOA and SOI technology seems to provide possibilities for improvements in both manufacture, e.g. reachable tolerances, and performance of imager sensor modules, e.g. lower power consumption.

CLAIMS:

1. A wafer scale package comprising:

a wafer with a sensor side, comprising a plurality of image sensor integrated circuits said image sensor integrated circuits having a photosensitive area located near said sensor side, comprising photosensitive elements for converting electromagnetic radiation to electric signals,

a solid spacer layer being arranged over said sensor side of said wafer, having a plurality of openings corresponding to the photosensitive areas, said openings preferably having at least the same areal dimensions as said photosensitive areas,

a transparent cover layer being arranged over said spacer layer.

2. A wafer scale package according to claim 1 comprising a further transparent cover layer being arranged over said transparent cover layer.

3. A wafer scale package according to claim 2 comprising a further spacer layer being arranged between said transparent cover layer and said further transparent cover layer, said further spacer layer having a plurality of further openings corresponding to the photosensitive areas, said further openings having at least the same areal dimensions as said photosensitive areas.

4. A wafer scale package according to claim 1, 2, or 3 wherein at least one of said cover layers comprises optical means arranged for modulating electromagnetic radiation traveling through said optical means to said photosensitive areas, preferably said optical means comprises a plurality of lenses, each of said lenses corresponding to one of said photosensitive areas.

5. A wafer scale package according to claim 4, wherein said further cover layer comprises a plurality of lens holders and optical means each of said lens holders and optical means corresponding to one of said photosensitive areas.

6. A wafer scale package according to claim 5, wherein said optical means comprise a lens.

7. A wafer scale package according to claim 1, 2, or 3, wherein an diaphragm layer is arranged over one of said cover layers, said diaphragm layer comprising a plurality of diaphragms corresponding to said plurality of photosensitive areas.

8 A wafer scale package according to claim 7, wherein said diaphragm layer is arranged over said further cover layer.

9. A wafer scale package according to claim 1, 2, or 3, wherein at least one of said spacer layers is made of glass, plastic, or metal.

10. A wafer scale package according to claim 1, 2, 3 or 9, wherein said openings have been made by powder blasting, ultrasonic drilling, or etching.

11. A wafer scale package according to claim 1, 2, or 3, wherein at least one of said cover layers is made of glass.

12. A wafer scale package according to claim 11, wherein said glass of at least one of said cover layers has infra red blocking properties.

13. A wafer scale package according to claim 11, wherein said glass of at least one of said cover layers is coated with an infra red blocking coating.

14. A wafer scale package according to claim 1, 2, 3, or 11 wherein at least one of said cover layers has been formed by powder blasting, ultrasonic drilling, etching, stamping, or hot glass molding.

15. A wafer scale package according to one of the preceding claims wherein said layers are mounted together with an adhesive.

16. A camera module comprising:
a semiconductor material die with a sensor side, comprising an image sensor

circuit, said image sensor integrated circuit having a photosensitive area located near said sensor side, comprising photosensitive elements for converting electromagnetic radiation to electric signals,

a solid spacer layer being arranged over said sensor side of said die, having an opening corresponding to said photosensitive area, said opening preferably having at least the same areal dimensions as said photosensitive area,

a transparent cover layer being arranged over said spacer layer.

17. A camera module according to claim 16, comprising a plurality of micro lenses arranged over said photosensitive area, each micro lens out of said plurality of micro lenses corresponding to one of said photosensitive elements.

18. A camera module according to claim 16 comprising a further transparent cover layer being arranged over said transparent cover layer.

19. A camera module according to claim 18 comprising a further spacer layer being arranged between said transparent cover layer and said further transparent cover layer, said further spacer layer having a further opening corresponding to said photosensitive area, said opening having at least the same areal dimension as said photosensitive area.

20. A camera module according to claim 16, 18, or 19 wherein at least one of said cover layers comprises optical means arranged for modulating electromagnetic radiation traveling through said optical means to said photosensitive areas.

21. A camera module according to claim 20, wherein said further cover layer comprises a lens holder and optical means, said lens holders and optical means corresponding to said photosensitive area.

22. A camera module according to claim 20 or 21, wherein said optical means comprise a lens.

23. A camera module according to claim 16, 18, or 19, wherein an diaphragm layer is arranged over one of said cover layers, said diaphragm layer comprising a diaphragm corresponding to said photosensitive area.

24. A camera module according to claim 23, wherein said diaphragm layer is arranged over said further cover layer.

25. A camera module according to claim 16, 18, or 19, wherein at least one of said spacer layers is made of glass, plastic, or metal.

26. A camera module according to claim 16, 18, 19 or 25, wherein said opening has been made by powder blasting, ultrasonic drilling, or etching.

27. A camera module according to claim 16, 18, or 19, wherein at least one of said cover layers is made of glass.

28. A camera module according to claim 27, wherein said glass of at least one of said cover layers has infra red blocking properties.

29. A camera module according to claim 27, wherein said glass of at least one of said cover layers is coated with an infra red blocking coating.

30. A camera module according to claim 16, 18, 19, or 27 wherein at least one of said cover layers has been formed by powder blasting, ultrasonic drilling, etching, stamping, or hot glass molding.

31. A camera module according to one of the claims 16 to 30 wherein said layers are mounted together with an adhesive.

32. A camera system with a camera module comprising:

a semiconductor material die with a sensor side, comprising an image sensor circuit, said image sensor integrated circuit having a photosensitive area located near said sensor side, comprising photosensitive elements for converting electromagnetic radiation to electric signals,

a solid spacer layer being arranged over said sensor side of said die, having an opening corresponding to said photosensitive area, said opening preferably having at least the

same areal dimensions as said photosensitive area,

a transparent cover layer being arranged over said spacer layer.

33. A method of manufacturing a camera module comprising a semiconductor material die with a sensor side, comprising an image sensor integrated circuit having a photosensitive area near said sensor side, said photosensitive area comprising photosensitive elements for converting electromagnetic radiation into electric signals, said method comprising:

a separation step of separating said die from a wafer,

said separation step being preceded by a spacer layer arranging step of arranging a solid spacer layer over said sensor side of said die, said solid spacer layer having an opening corresponding to said photosensitive area, said opening preferably having at least the same real dimensions as said photosensitive area

said spacer layer arranging step being followed by a step of arranging a transparent cover layer over said spacer layer.

34. A method of manufacturing a camera module according to claim 33, said layers having substantially the same shape as said wafer.

35. A method of manufacturing a camera module according to claim 33 or 34, said method comprising a step of mounting together said layers by gluing with an adhesive.

36. A method of manufacturing a solid spacer layer for use in a wafer scale package, said method comprising a step of forming an array of openings in said spacer layer.

37. A method according to claim 36, said spacer layer being made of glass, plastic, or metal.

38. A method according to claim 36 or 37, said openings being formed by powder blasting, ultrasonic drilling, or etching.

39. A method of manufacturing a transparent cover layer for use in a wafer scale package, said method comprising a step of forming an array of lenses in said cover layer.

40. A method according to claim 39, said cover layer being made of glass.

41. A method according to claim 39 or 40, said cover layer being formed by powder blasting, ultrasonic drilling, etching, stamping, or hot glass molding.

ABSTRACT:

A camera module comprising a solid state image sensor (SSIS) and improved manufacture thereof are introduced. The SSIS comprises a semiconductor substrate layer, in which electrical functional circuitry is integrated. Said semiconductor substrate layer provides a sensor side with at least one photosensitive area. Over said sensor side a stack of different layers is arranged, wherein said stack comprises at least one first transparent layer arranged over said sensor side, at least one second transparent layer being arranged over said first transparent layer comprising optical means for modulating of electromagnetic radiation traveling through said optical means to said photosensitive area, and at least one spacer layer arranged between said sensor side surface and said second transparent layer, wherein said spacer layer provides a through hole coinciding with said photosensitive area and having at least same areal dimensions and shape as said photosensitive area.

Fig. 4e

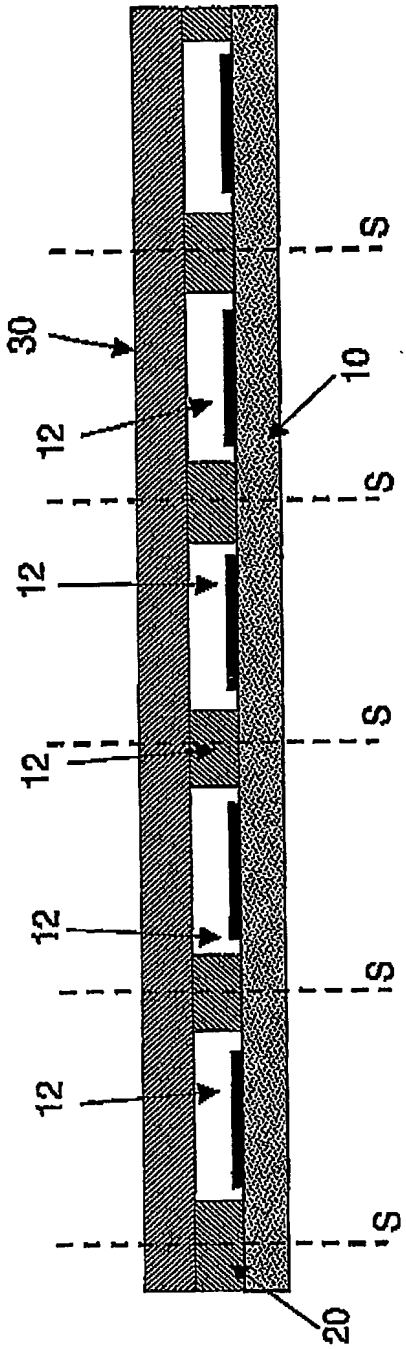

FIG.1

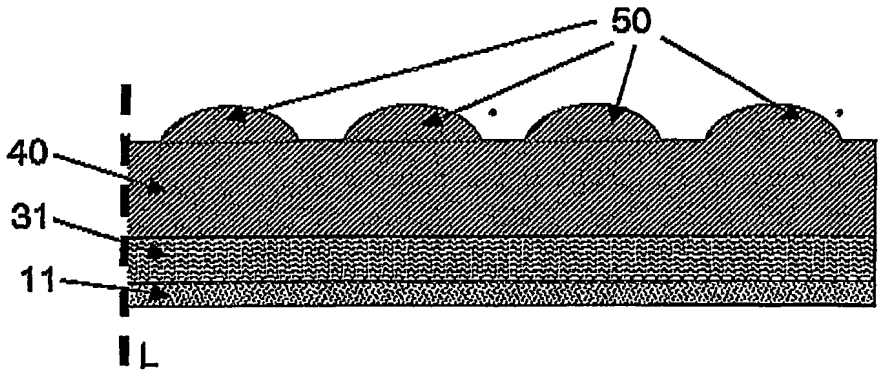

FIG.2a

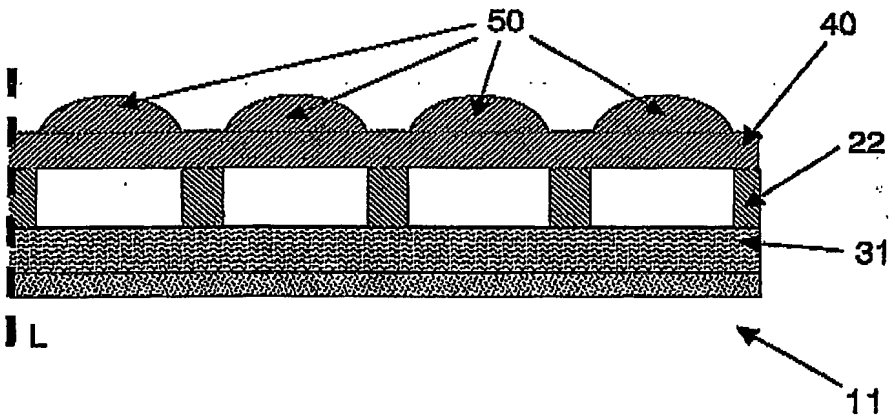

FIG.2b

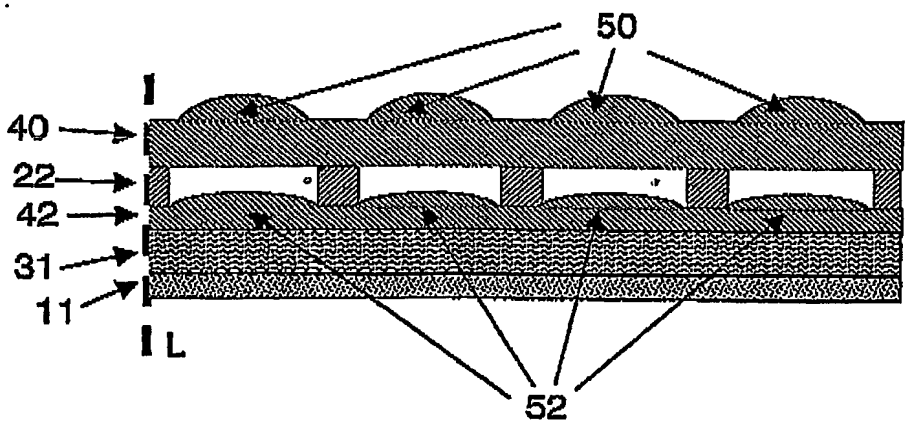

FIG.2c

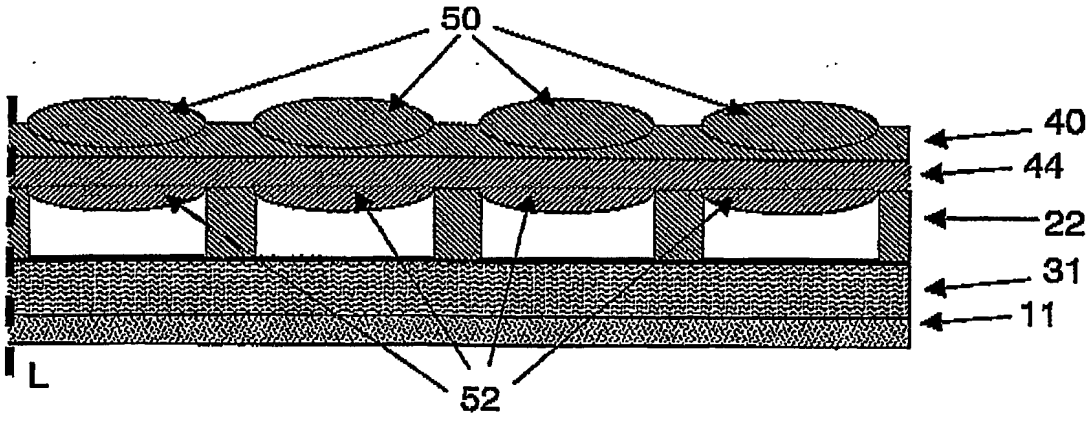

FIG.2d

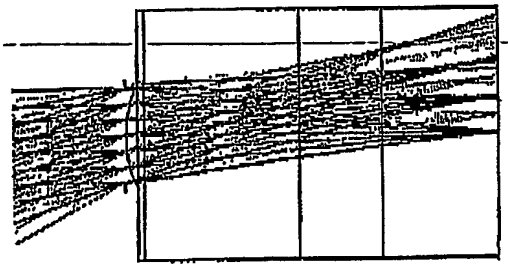

FIG.3a

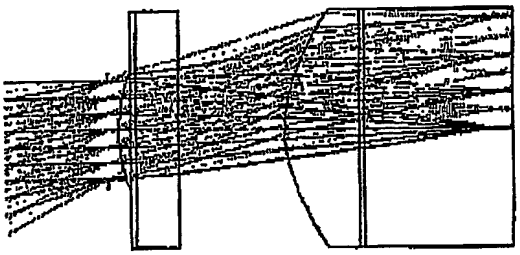

FIG.3b

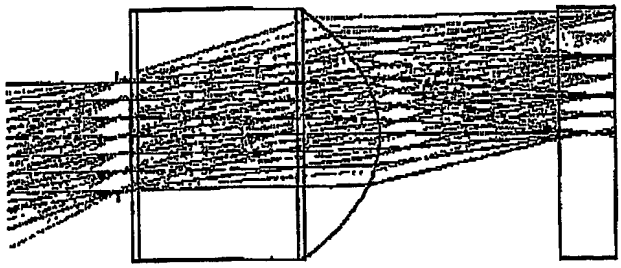

FIG.3c

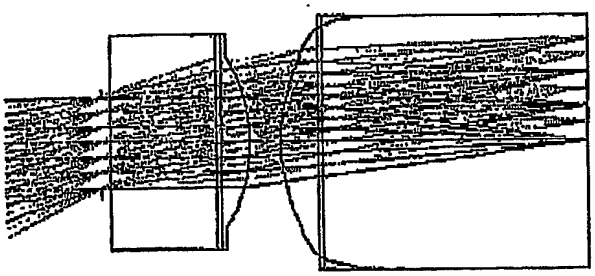

FIG.3d

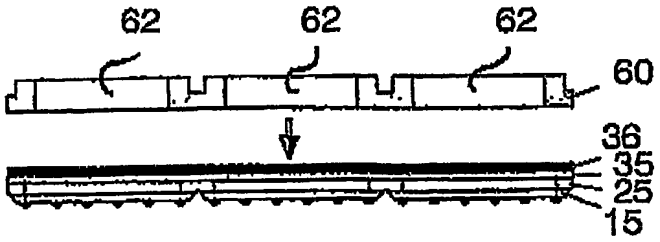

FIG.4a

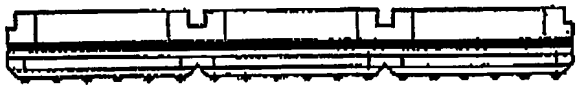

FIG.4b

FIG.4c

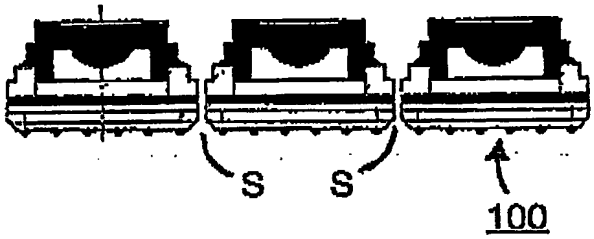

FIG.4d

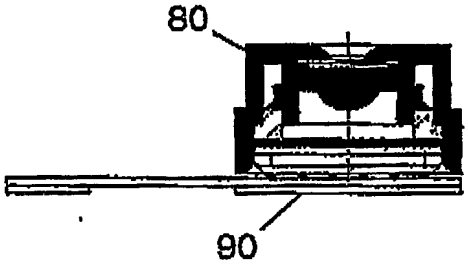

FIG.4e